Radiation Hardened Adjustable Positive Voltage Regulator

HS-117RH, HS-117EH

The radiation hardened HS-117RH and HS-117EH are adjustable positive voltage linear regulators capable of operating with input voltages up to 40VDC. The HS-117EH encompasses all of the production testing of the HS-117RH and additionally is tested in the Intersil Enhanced Low Dose Rate Sensitivity (ELDRS) product manufacturing flow. The output voltage is adjustable from 1.25V to 37V with two external resistors. The device is capable of sourcing from 5mA to 1.25A max (0.5A max for the TO-39 package). Current protection is provided by the on-chip thermal shutdown and output current limiting circuitry.

The Intersil HS-117 has advantages over other industry standard types, in that circuitry is incorporated to minimize the effects of radiation and temperature on device stability.

Constructed in Intersil's dielectrically isolated Rad Hard Silicon Gate (RSG) process, the HS-117RH and HS-117EH are immune to single event latch-up and has been specifically designed to provide highly reliable performance in harsh radiation environments.

Applications

- Adjustable Voltage Regulators
- Adjustable Current Regulators

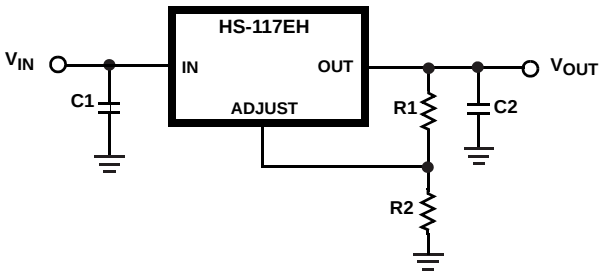
Features

- Electrically screened to DLA SMD # 5962-99547
- Superior temperature stability
- Overcurrent and Over-temperature protection
- Wide input voltage range . . . . . 4.25V to 40V
- Operating temperature range. . . . . -55°C to +125°C
- QML Qualified per MIL-PRF-38535 requirements
- Radiation environment
  - SEL/SEB LET_{TH} (V_S = ±20V). . . . . 87.4 MeV•cm^2/mg
  - Total Dose, High Dose Rate . . . . . 300krad(Si)
  - Total Dose, Low Dose Rate . . . . . 100krad(Si)*

* Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

Related Literature

- TID, "Total Dose Testing of the HS117 Linear Regulator"
- SEE, "SEE Testing of the HS117 Linear Regulator"
- ELDRS, "Low Dose Testing of HS117 to 100krad(Si)"



$V_{OUT} = V_{REF} (1+R2/R1) + I_{ADJ} R2$

FIGURE 1. TYPICAL APPLICATION

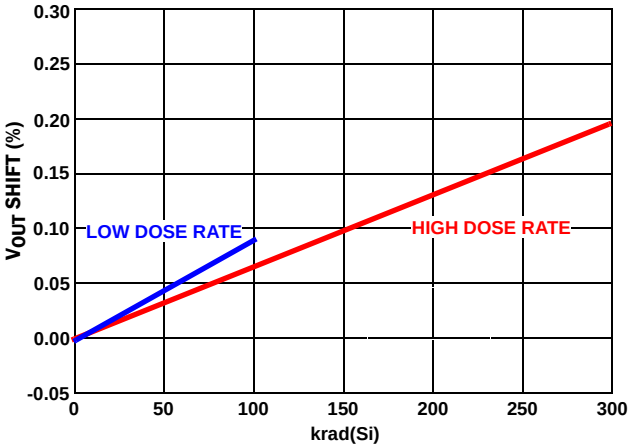


FIGURE 2. V_{OUT} SHIFT vs HIGH and LOW DOSE RATE RADIATION

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

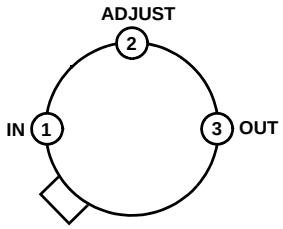
ORDERING SMD NUMBER (Note 2)	INTERNAL MKTG. PART NUMBER	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9954702V9A	HS0-117EH-Q	-55 to +125	DIE	
5962F9954701V9A	HS0-117RH-Q	-55 to +125	DIE	
HS0-117RH/SAMPLE	HS0-117RH/SAMPLE	-55 to +125	DIE	
5962F9954702VUC	HS2-117EH-Q (Note 1)	-55 to +125	3 Ld METAL CAN	T3.C
5962F9954701VUC	HS2-117RH-Q (Note 1)	-55 to +125	3 Ld METAL CAN	T3.C
5962F9954701QUC	HS2-117RH-8 (Note 1)	-55 to +125	3 Ld METAL CAN	T3.C
HS2-117RH/PROTO	HS2-117RH/PROTO (Note 1)	-55 to +125	3 Ld METAL CAN	T3.C
5962F9954702VYC	HSYE-117EH-Q (Note 1)	-55 to +125	3 PAD CLCC	J3.A
5962F9954701VYC	HSYE-117RH-Q (Note 1)	-55 to +125	3 PAD CLCC	J3.A
5962F9954701QYC	HSYE-117RH-8 (Note 1)	-55 to +125	3 PAD CLCC	J3.A
HSYE-117RH/PROTO	HSYE-117RH/PROTO (Note 1)	-55 to +125	3 PAD CLCC	J3.A
5962F9954701VXC	HS9S-117RH-Q (Note 1)	-55 to +125	3 Ld TO-257	T3.D
5962F9954701QXC	HS9S-117RH-8 (Note 1)	-55 to +125	3 Ld TO-257	T3.D
5962F9954702VXC	HS9S-117EH-Q (Note 1)	-55 to +125	3 Ld TO-257	T3.D
HS9S-117RH/PROTO	HS9S-117RH/PROTO (Note 1)	-55 to +125	3 Ld TO-257	T3.D

NOTES:

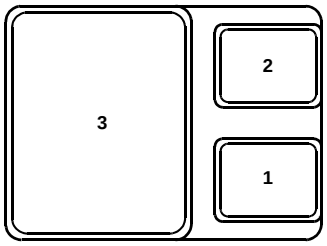
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table on page 2 must be used when ordering.

Pin Configurations

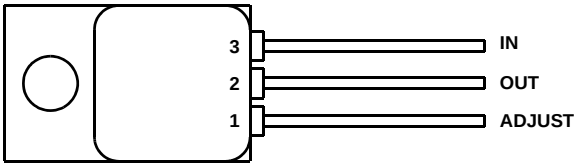
HS2-117RH
(TO-39 CAN)
BOTTOM VIEW



HSYE-117RH
(SMD.5 CLCC)
BOTTOM VIEW



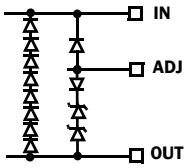
HS9S-117RH
(TO-257AA FLANGE MOUNT)
TOP VIEW



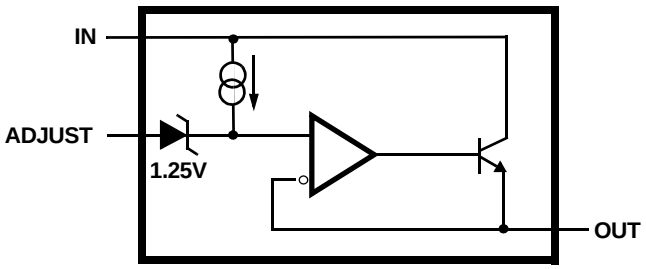
NOTE: No current JEDEC outline for the SMD.5 package. Refer to SMD for package dimensions. The TO-257 is a totally isolated metal package.

Pin Descriptions

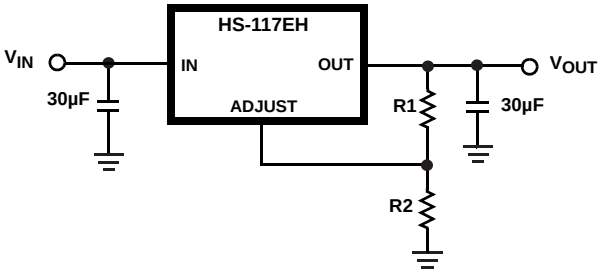
HS2-117RH (TO-39)	HS9S-117RH (TO-257AA)	HSYE-117RH (SMD.5 CLCC)	PIN NAME	DESCRIPTION
1	3	2	IN	Regulator Input
2	1	1	ADJUST	Voltage Adjust Feedback Input
3	2	3	OUT	Regulator Output



Functional Block Diagram

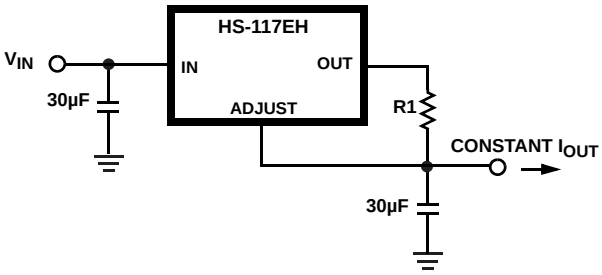


Typical Applications



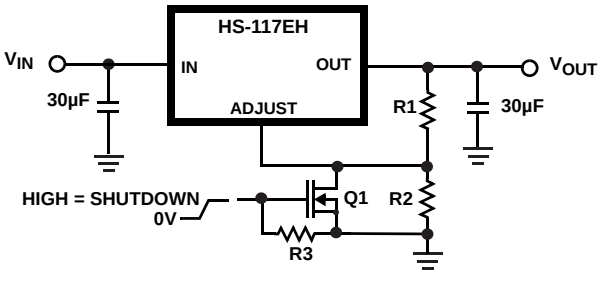
$V_{OUT} = V_{REF} (1+ R2/R1) + I_{ADJ}*R2$

FIGURE 3. RESISTOR ADJUSTED OUTPUT VOLTAGE



$I_{OUT} = V_{REF} / R1$

FIGURE 4. CONSTANT CURRENT REGULATOR



In shutdown $V_{OUT} = V_{REF}$

FIGURE 5. REGULATOR SHUTDOWN

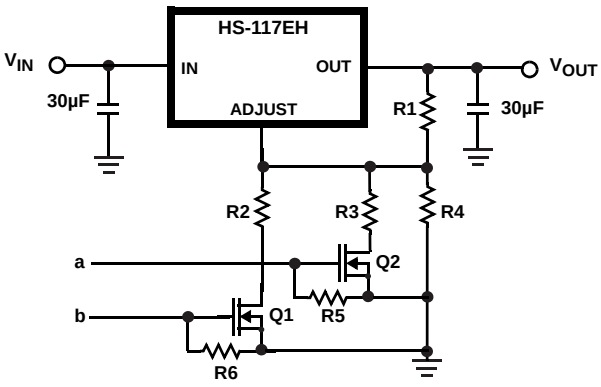


FIGURE 6. FOUR DIGITALLY PROGRAMMED OUTPUT VOLTAGES

Absolute Maximum Ratings

Input to Output Voltage Differential 40V
Input to Output Voltage Differential (Note 5) 40V
Maximum Output Current 1.5A

Maximum Power Dissipation T_C = +25°C
HS2-117 (TO-39 Can) 8W
HS9S-117 (TO-257AA Flange Mount) 50W
HSYE-117 (SMD.5 CLCC) 27.5W
Maximum Power Dissipation T_C = +100°C (Note 6)
HS2-117 (TO-39 Can) 3.3W
HS9S-117 (TO-257AA Flange Mount) 20W
HSYE-117 (SMD.5 CLCC) 11W

ESD Rating
Human Body Model (HBM) (Tested per MIL-PRF-883 3015.7) . . . 1500V
Machine Model (MM) (Tested per EIA/JESD22-A115-A) 350V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TO-39 (Notes 3, 4, 6)	125	15
TO-257AA (Notes 3, 4, 6)	26	2.5
SMD.5 (Notes 3, 4, 6)	42	4.5

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +175°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Input Voltage Range . . . . . 4.25V to 40V
Output Voltage Range . . . . . 1.25V to 37V
Minimum Output Current 5mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. The maximum supply limit specified is for operation in a heavy ion environment at an LET = 87.4MeV*cm^2/mg.
6. The linear derating factor for TO-39 package is 0.067 W/°C, for TO-257AA package is 0.4 W/°C, for the SMD.5 package is 0.22 W/°C

Electrical Specifications

V_{DIFF} = 3V, T_A = 25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{REF}	Reference Voltage	V_{DIFF} = 3V, V_{DIFF} = 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA	**1.20**	1.255	**1.30**	V
R_{LINE}	Line Regulation	V_{REF} = V_{OUT} - V_{ADJ}, 3V ≤ V_{DIFF} ≤ 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA	**-0.02**	0.005	**0.02**	%
R_{LOAD}	Load Regulation	V_{DIFF} = 3V, 5mA ≤ I_{OUT} ≤ 1.25A TO-257AA and SMD.5 packages only	**-1.5**	-0.1	**1.5**	%
		V_{DIFF} = 3V, 5mA ≤ I_{OUT} ≤ 500mA TO-39 package	**-1.5**	-0.8	**1.5**	%
I_{ADJ}	Adjust Pin Current	V_{DIFF} = 3V, V_{DIFF} = 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA		64	**100**	µA
dI_{ADJ}	Adjust Pin Current Change	3V I_{ADJ} - 40V I_{ADJ} 5.0mA ≤ I_{OUT} ≤ 5.5mA	**-6**	2.36	**6**	µA
I_{OUT}	Maximum Output Current	TO-257AA and SMD.5 packages only	**1.25**			A
		TO-39 package	**0.5**			A
T_{ON}	V_{IN} Applied to V_{OUT} Turn-on			0.2		ms
I_{sc}	Max. Output Short Circuit Current Limit	V_{OUT} = 0V		3		A
OT	Over-temperature Shutdown			150	**175**	°C
OT_HYS	Over-temperature Hysteresis			20		°C

Post Radiation Electrical Specifications

V_{DIFF} = 3V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300krad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure a low dose rate of <10mrad(Si)/s.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 7)	MAX (Note 7)	UNITS
V_{REF}	Reference Voltage	V_{DIFF} = 3V, V_{DIFF} = 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA	**1.20**	**1.30**	V
R_{LINE}	Line Regulation	$V_{REF} = V_{OUT}-V_{ADJ}$, 3V ≤ V_{DIFF} ≤ 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA	**-0.02**	**0.02**	%
R_{LOAD}	Load Regulation	V_{DIFF} = 3V, 5mA ≤ I_{OUT} ≤ 1.25A TO-257AA and SMD.5 packages only	**-1.5**	**1.5**	%
		V_{DIFF} = 3V, 5mA ≤ I_{OUT} ≤ 500mA TO-39 package	**-1.5**	**1.5**	%
I_{ADJ}	Adjust Pin Current	V_{DIFF} = 3V, V_{DIFF} = 40V, 5.0mA ≤ I_{OUT} ≤ 5.5mA		**100**	µA
dI_{ADJ}	Adjust Pin Current Change	3V I_{ADJ} - 40V I_{ADJ} 5.0mA ≤ I_{OUT} ≤ 5.5mA	**-6**	**6**	µA
I_{OUT}	Output Current	TO-257AA and SMD.5 packages only	**1.25**		A
		TO-39 package	**0.5**		A

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Post Radiation Characteristics This data is a typical mean test data post total dose radiation exposure at both a low dose rate (LDR) of <10mrad(Si)/s to 100krad(Si) and at a high dose rate (HDR) of 50 to 300rad(Si)/s to 300krad(Si). This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

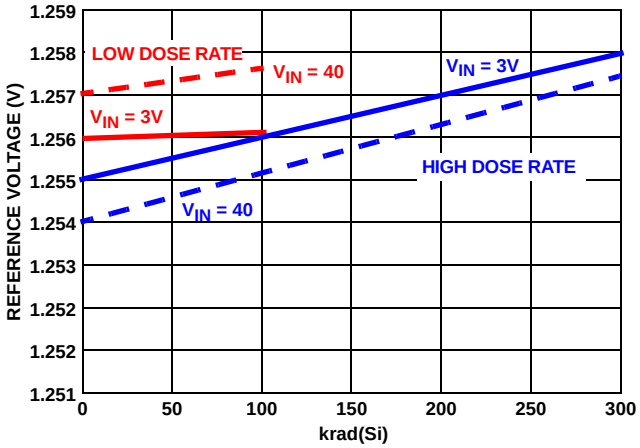


FIGURE 7. REFERENCE VOLTAGE vs RADIATION

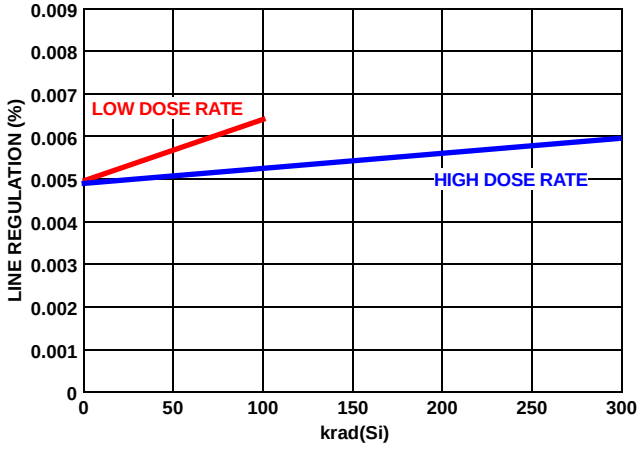


FIGURE 8. LINE REGULATION (3V ≤ V_{DIFF} ≤ 40V) vs RADIATION

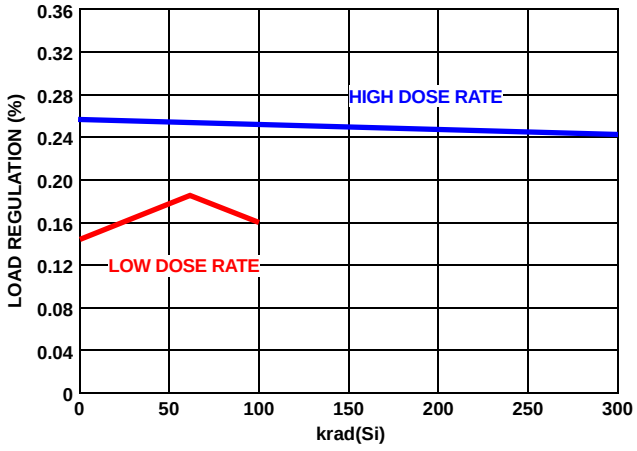


FIGURE 9. LOAD REGULATION (I_{OUT} 5mA to 1.25A) vs RADIATION

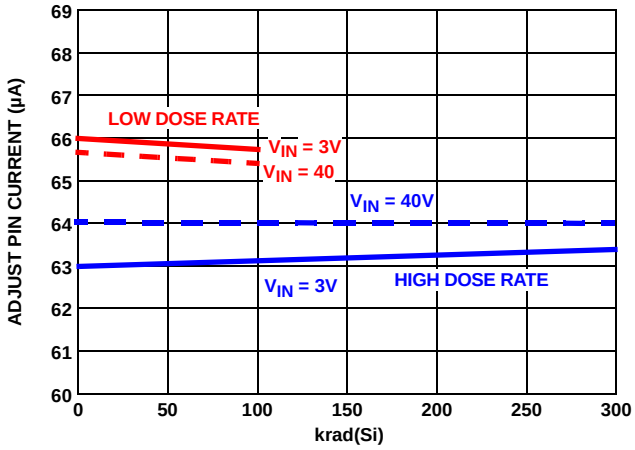


FIGURE 10. ADJUST PIN CURRENT vs RADIATION

Typical Performance Curves

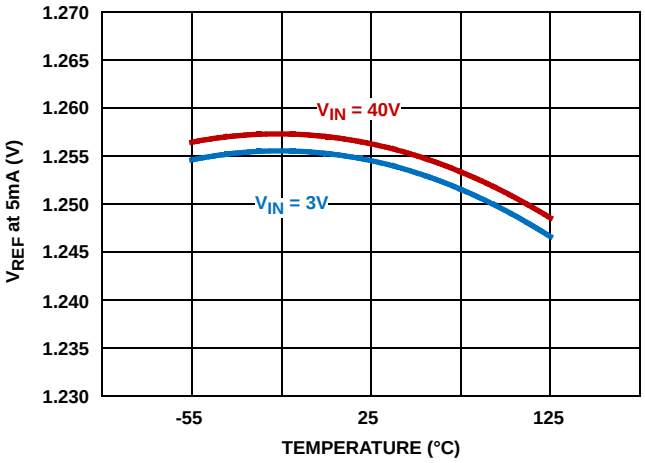


FIGURE 11. V_{REF} vs TEMPERATURE

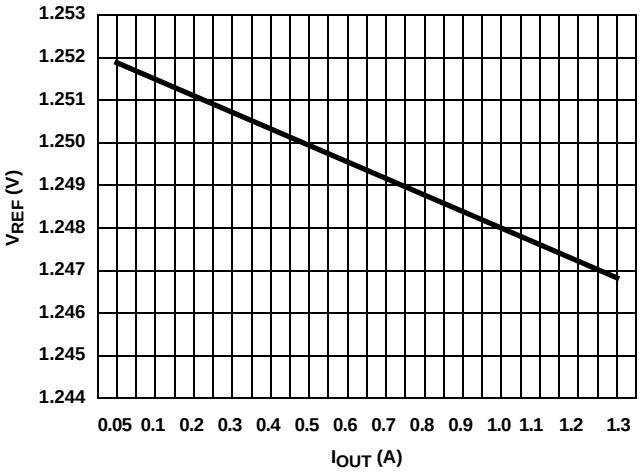


FIGURE 12. V_{REF} vs OUTPUT CURRENT at T_A = +25°C

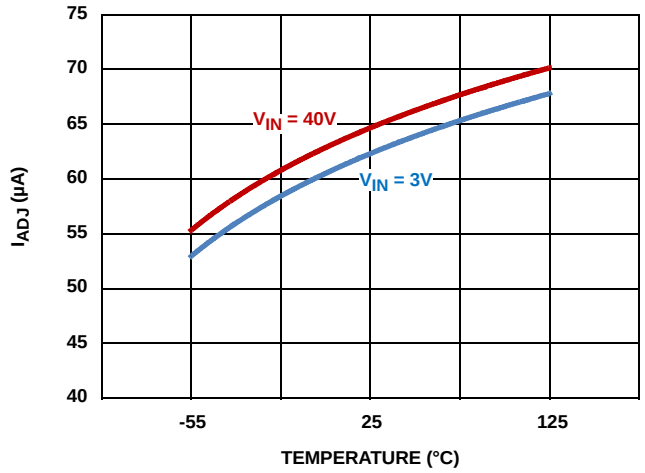


FIGURE 13. I_{ADJ} vs TEMPERATURE

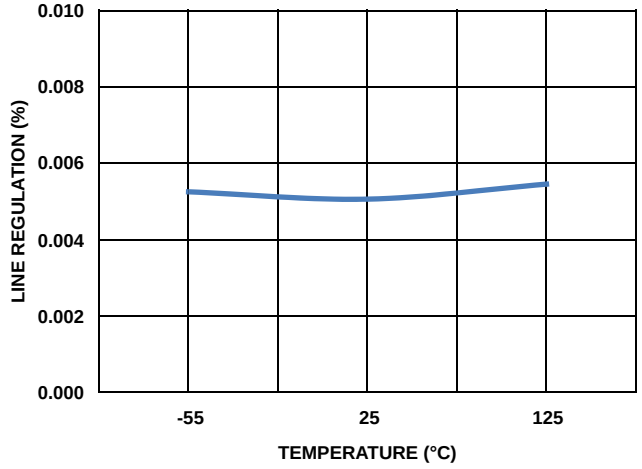


FIGURE 14. LINE REGULATION vs TEMPERATURE

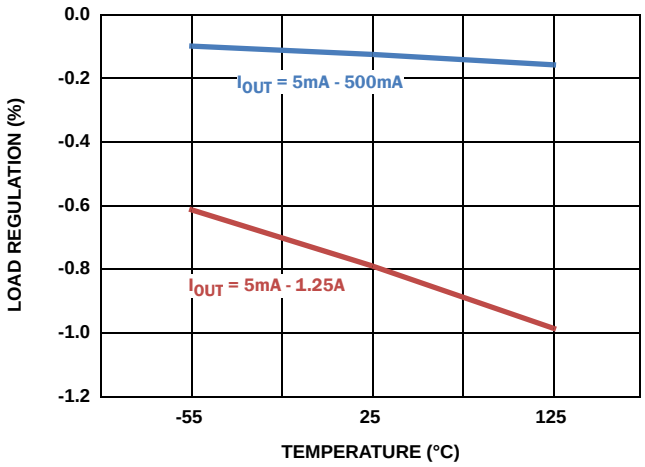


FIGURE 15. LOAD REGULATION vs TEMPERATURE

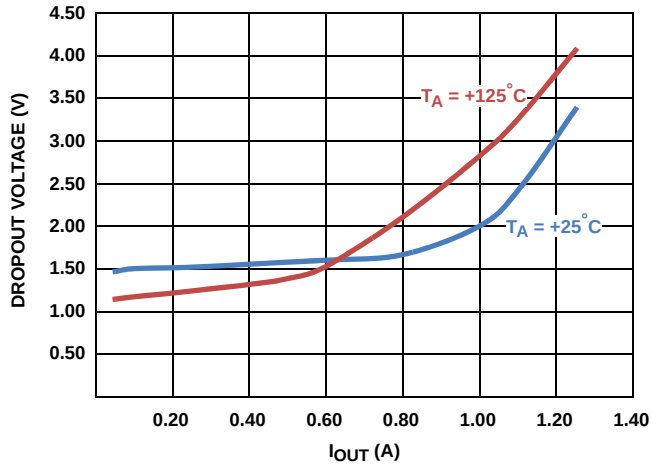


FIGURE 16. DROPOUT VOLTAGE vs OUTPUT CURRENT, V_{IN} = 12V

Typical Performance Curves (Continued)

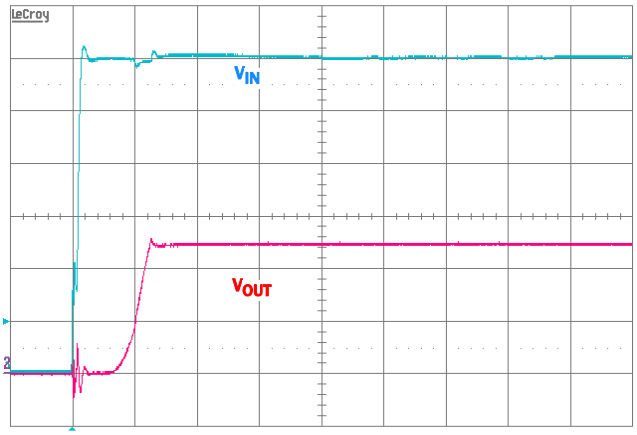


FIGURE 17. POWER-ON V_{IN} = 12V, V_{OUT} = 5V, RI = 10Ω

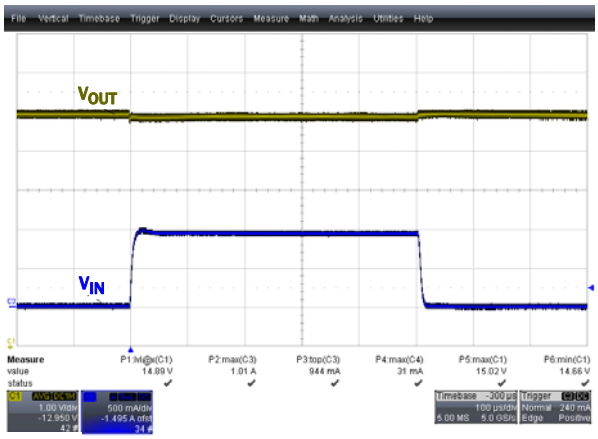


FIGURE 18. V_{IN} = 30V, V_{OUT} = 15V, I_{OUT} 0 -1A STEP

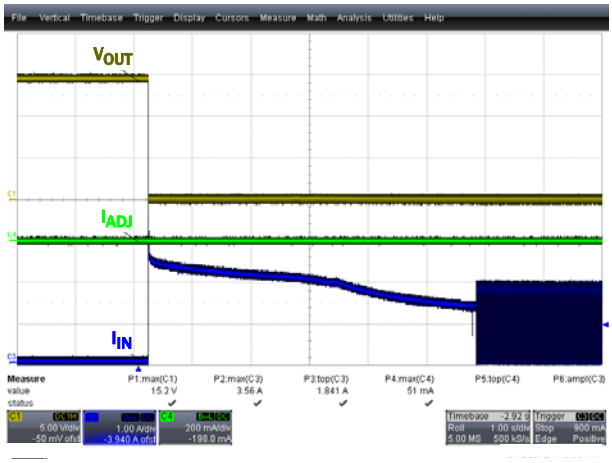


FIGURE 19. SHORT CIRCUIT INTO OVER-TEMP PROTECTION

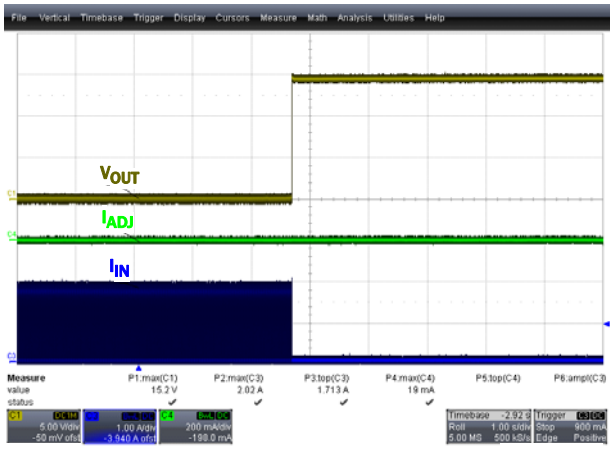


FIGURE 20. SHORT CIRCUIT RECOVERY

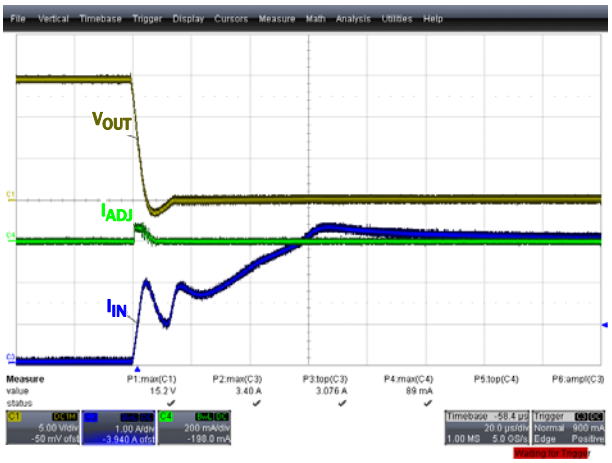


FIGURE 21. SHORT CIRCUIT CURRENT LIMIT DETAIL

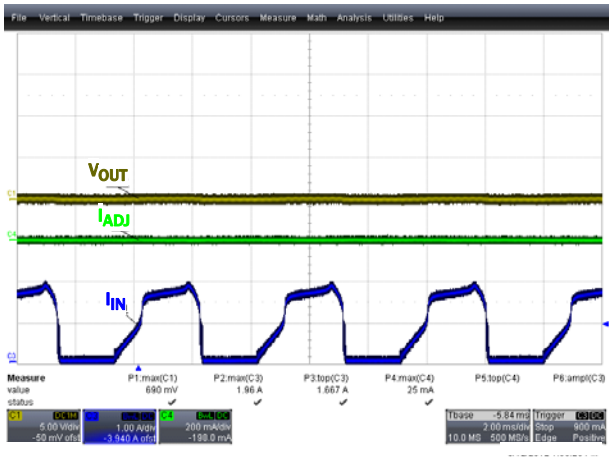


FIGURE 22. SHORT CIRCUIT OVER-TEMP PROTECTION DETAIL

Functional Description

Functional Overview

The radiation hardened HS-117RH, HS-117EH are adjustable positive voltage linear regulators capable of operating with input voltages up to 40 VDC. The output voltage is adjustable from 1.25V (V_{REF}) to 37V with two external resistors. The device is capable of sourcing from 5mA to 1.25A_{PEAK} (0.5A_{PEAK} for the TO-39 can package). Dual mode protection is provided by the on-chip +175^{o}C thermal shutdown at output current limiting circuitry.

The Intersil HS-117RH, HS-117EH has advantages over other industry standard types, in that circuitry is incorporated to minimize the effects of radiation and temperature on device stability providing < 0.2% shifts in output voltage over 300krad(Si) of high dose rate (HDR) and 100krad(Si) of low dose rate (LDR) gamma radiation.

Constructed with the Intersil dielectrically isolated Radiation Hardened Silicon Gate (RSG) process, the HS-117RH and HS-117EH are both immune to single event latch-up and have been specifically designed to provide highly reliable performance providing power in harsh radiation environments.

Output Voltage Adjustment

The HS-117 is an adjustable output voltage regulator operating with a 1.25V reference voltage developed between the OUT and ADJUST pins. The ADJ current (I_{ADJ}) is typically 64µA at +25°C and 100µA maximum over temperature.

Linear regulators typically need a minimum current load for the regulation amplifier feedback to maintain stability, and for the HS-117 this minimum is 5mA. In order to ensure stability in all situations, the minimum resistor between the VOUT and ADJ is suggested to be 120 Ω.

Referring to Figure 1, the reference voltage is programmed to a constant current source by resistor R1, and this current flows through R2 to ground to set the output voltage, see Equation 1.

$$V_{OUT} = 1.25(1 + R2/R1) + I_{ADJ}R2 \quad \text{(EQ. 1)}$$

In practical applications the R2 value is in the range of a few kΩ, so that the I_{ADJ} x R2 contribution can be ignored in the V_{OUT} calculation; simplifying the V_{OUT} calculation to the following:

$$V_{OUT} = 1.25(1 + R2/R1) \quad \text{(EQ. 2)}$$

CURRENT LIMITING

The HS-117 has internal current limiting that will be activated whenever the output current exceeds the lower limit of the Maximum Output Current parameter shown in the “Electrical Specifications” on page 5, (typically limiting to ~1.5A) to a maximum limit of typically 3A in an output short circuit condition.

During a short circuit condition if the regulator's differential voltage exceeds the Absolute Maximum Rating of 40V (e.g. $V_{IN} \geq$ 40V, V_{OUT} = 0V), the device may be likely damaged.

Performance and PCB Layout Considerations

In order to optimize load regulation performance, it is important to implement Kelvin connections for the R1 and R2 resistors. In practice, the R1 connection must be close to the OUT and ADJUST pins. This is done to eliminate PCB trace resistance being included in the constant current determination. In contrast, the R2 to ground connection must be placed as near as possible to the negative load pin to ensure that the voltage being delivered to the load is as designed for by the choice of R1 and R2 values.

Ripple rejection can be improved by placing a 10µF capacitor across the R2 resistor. At low output voltage, increasing this capacitor value will further decrease output ripple.

External Bypass Capacitors

Input bypass capacitance is recommended to enhance regulator stability if the device is located more than a few inches from its power source. The input bypass capacitor (C1) should be mounted with the shortest possible track length directly across the regulator’s input and ground terminals. A 30µF tantalum capacitor should be adequate for most applications. Frequency compensation for the regulator is provided by the output capacitor (C2) and is required to ensure output stability. A minimum (C2) capacitance value of 30µF is recommended. Higher values of output capacitance can be used to enhance loop stability, transient response and output noise.

Thermal Considerations

The HS-117 has a thermal limiting circuit that is designed to protect the regulator when the junction temperature is typically > +150°C. The regulator output turns off and then on again as the die cools. If the device is continuously operated in an over-temperature condition, this feature provides protection from catastrophic device damage due to accidental or prolonged overheating.

The HS-117 is available in a TO-39 3 pin can, a TO-257AA flange mount and a SMD.5 CLCC surface mount packages. These packages represent a wide range of thermal resistance to the die and thus a wide range of power dissipation (P_D) capabilities. Consult the “Thermal Information” on page 5 for the relevant package thermal impedances. Also the “Absolute Maximum Ratings” on page 5 lists the power dissipation limitations by package.

When developing circuits using the HS-117, its thermal performance and limitations should be tested in order to insure acceptable performance. As with all tabbed packaged devices, flange mounting to a thermal heat-sink is recommended for the TO-257AA following best practices.

T0-257AA Package Characteristics

Weight of Packaged Device

4.50 Grams (Typical)

Case Characteristics

Finish: Gold
Potential: Unbiased

T0-39 Package Characteristics

Weight of Packaged Device

0. 91 Grams (Typical)

Case Characteristics

Finish: Steel, Gold
Potential: Unbiased

SMD.5 CLCC Package Characteristics

Weight of Packaged Device

0.91 Grams (Typical)

Case Characteristics

Finish: Gold, Ceramic
Potential: Unbiased

Die Characteristics

Die Dimensions

2616µm x 2794µm (103mils x 110mils)
Thickness: 483µm ± 25µm (19mils ± 1mil)

Interface Materials

GLASSIVATION

Type: PSG
Thickness: 8kÅ ± 1kÅ

TOP METALLIZATION

Type: Al/Cu/Si (98.75%/0.5%/0.75%)
Thickness: 16kÅ

BACKSIDE FINISH

Gold

Assembly Related Information

SUBSTRATE POTENTIAL

Unbiased (DI)

Additional Information

WORST CASE CURRENT DENSITY

$< 2 \times 10^5$ A/cm^2

PROCESS

Dielectrically Isolated RH - Si-GATE

TRANSISTOR COUNT:

96

Metallization Mask Layout

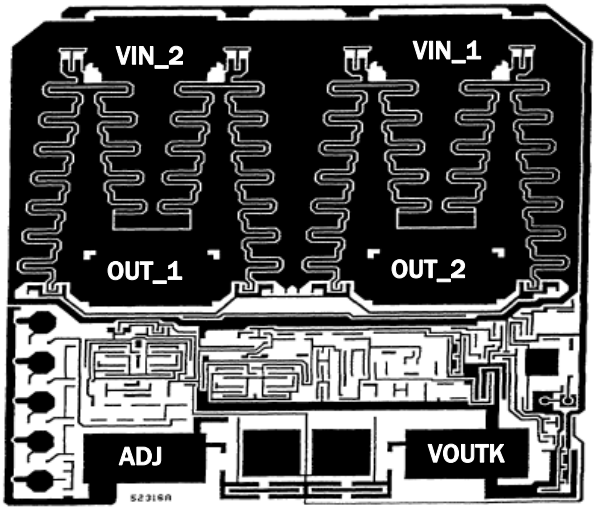


TABLE 1. DIE LAYOUT X-Y COORDINATES (Notes: 8, 9)

PAD NAME	X (µm)	Y (µm)	dX (µm)	dY (µm)
VIN_1	1214	2191	514	257
VIN_2	14	2191	514	257
VOUT_1	14	934	514	257
ADJ	0	0	514	257
VOUTK	1361	14	514	257
VOUT_2	1214	934	514	257

NOTES:

8. Origin of coordinates is the centroid of pad ADJ.
9. Bond Pads sized for is 5mil diameter wire

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
March 25, 2014	FN4560.10	Updated “Ordering Information on page 2. Expanded content in datasheet from 3 to 15 pages.
Sept 4, 2012	FN4560.9	Added HS-117EH as Device # to datasheet (EH FGs already added to the Ordering Information table), making this a 2-part datasheet: HS-117RH, HS-117EH. Global search/change HS-117RH to HS-117RH, HS-117EH.
Dec 15, 2011	FN4560.8	Added parts to datasheet: HS2-117EH-Q, HS0-117EH-Q, HS9S-117EH-Q and HSYE-117EH-Q
Oct 10, 2003	FN4560.7	Revised datasheet includes a new date and file number.

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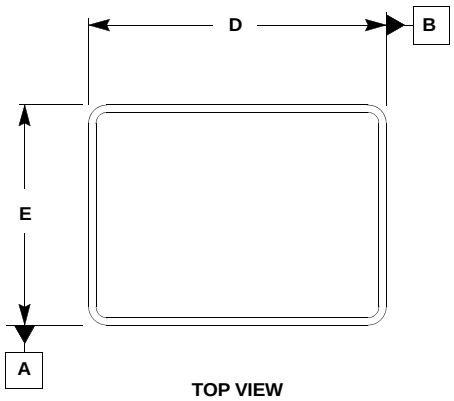
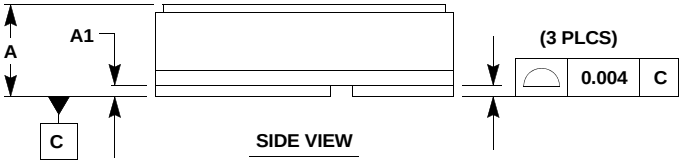
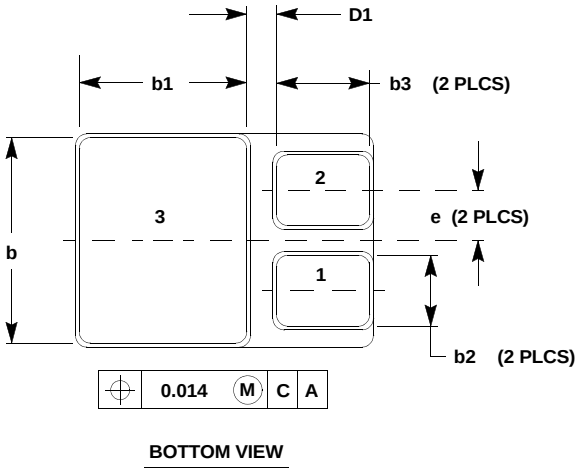
Ceramic Leadless Chip Carrier Packages (CLCC)







J3.A

3 PAD HERMETIC SMD.5 PACKAGE
CERAMIC BOTTOM TERMINAL CHIP CARRIER

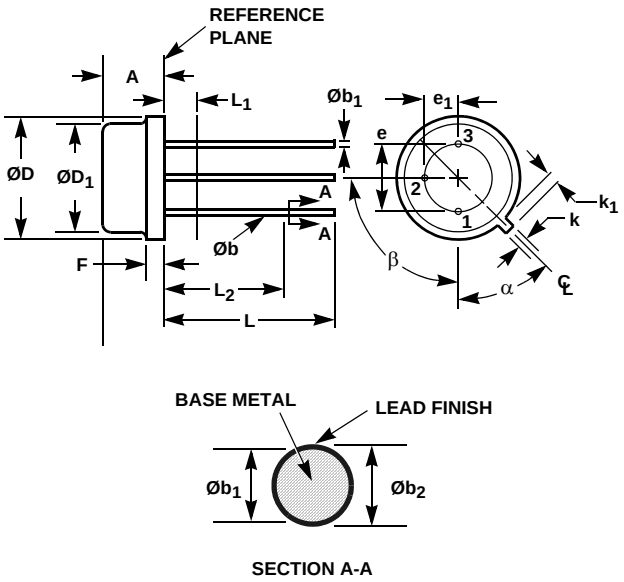
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.110	0.124	2.79	3.15	3
A1	0.010	0.020	0.25	0.51	-
b	0.281	0.291	7.13	7.39	-
b1	0.220	0.230	5.58	5.84	-
b2	0.090	0.100	2.28	2.54	-
b3	0.115	0.125	2.92	3.18	-
D	0.395	0.405	10.03	10.28	-
D1	0.030	-	0.76	-	-
E	0.291	0.301	7.39	7.64	-
e	0.075 BSC		1.91 BSC		-

Rev. 2 1/14

NOTES:

1. Controlling dimensions are in inches (mm for reference only).
2. Dimensioning and tollorance per ANSI Y14.5M - 1982
3. The maximum “A” dimension is package height before being solder dipped.
4. Patterned after MIL-STD-1835 CBCC1-N3 (C-B1) Note: Not meeting the Mil-Std “A” min. dimension of 0.112

Metal Can Package



T3.C

3 LEAD TO-39 (TO-205) METAL CAN PACKAGE

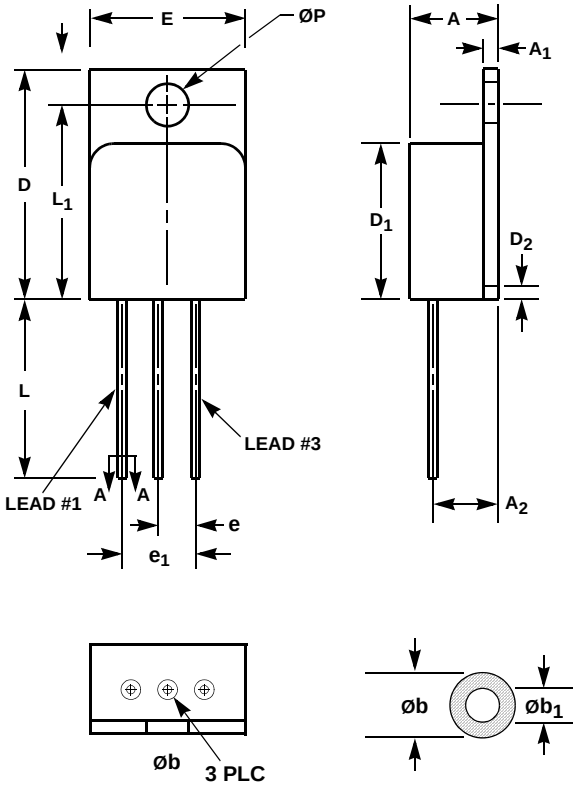
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.160	0.180	4.07	4.58	-
Øb	0.016	0.019	0.41	0.48	1
$Øb_1$	0.016	0.021	0.41	0.53	1
$Øb_2$	0.016	0.024	0.41	0.61	-
ØD	0.350	0.370	8.89	9.40	-
$ØD_1$	0.315	0.335	8.00	8.51	-
e	0.200 BSC		5.08 BSC		-
e_1	0.100 BSC		2.54 BSC		-
F	0.009	0.050	0.23	1.27	-
k	0.027	0.034	0.69	0.086	-
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1	-	0.050	-	1.27	1
L_2	0.250	-	6.35	-	1
α	45° BSC		45° BSC		3
β	90° BSC		90° BSC		-
N	3		3		4

Rev. 0 6/01

NOTES:

1. (All leads) Øb applies between L_1 and L_2. $Øb_1$ applies between L_2 and 0.500 from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Controlling dimension: Millimeter.

Hermetic Metal Package



T3.D

3 LEAD JEDEC TO-257AA HERMETIC METAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.200	4.78	5.08	7
A_1	0.035	0.045	0.89	1.14	-
A_2	0.120 BSC		3.05 BSC		-
D	0.645	0.665	16.39	16.89	-
D_1	0.410	0.430	10.41	10.92	-
D_2	-	0.038	-	0.97	-
e	0.100 BSC		2.54 BSC		-
e_1	0.200 BSC		5.08 BSC		-
E	0.410	0.420	10.41	10.67	-
Øb	0.025	0.040	0.64	1.02	1, 2
$Øb_1$	0.025	0.035	0.64	0.89	1, 2
L	0.500	0.750	12.70	19.05	-
L_1	0.527	0.537	13.39	13.64	-
P	0.140	0.150	3.56	3.81	-
N	3		3		5

Rev. 2 3/09

NOTES:

1. Dimension $Øb_1$ applies to base metal only. Dimension Øb applies to plated part.
2. Section A-A dimension apply between 0.100 inch (2.54mm) to 0.150 inch (3.81mm) from lead tip.
3. Die to base BeO isolated, terminals to case is plated.
4. Controlling dimensions are in inches (mm for reference only).
5. N is the maximum number of terminal positions.
6. Patterned after MIL-STD-1835 MSFM1-P3AA.
7. “A” minimum dimension not meeting the MIL-STD 0.190 minimum dimension.